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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/904,663	07/16/2001	Mikio Ohtaki	KAN 120D1	7934

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EXAMINER
HOLLINGTON, JERMELE M

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/904,663	OHTAKI, MIKIO	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-27 and 42-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-27 and 42-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/434,490* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's arguments, see remarks section on pages 3-5, filed April 10, 2003, with respect to claims 21-27 and 42-52 have been fully considered and are persuasive. The previous final rejection of claims 21-27 and 42-52 has been withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakata et al (6297658) in view of Budnaitis et al (5896038).

Regarding claim 21, Nakata et al discloses [see fig. 1] a method of manufacturing probe card of a wafer burn-in cassette comprising providing a semiconductor wafer (10) having a plurality of circuit elements [not shown] on a surface [not number but shown in fig. 1] thereof [see column 3 lines 27-30 and column 6 lines 25-26], forming on the wafer surface [not number but shown] a plurality of electrodes (16) connected with the circuit elements [see column 6 lines 30-31], coating the wafer surface with a resin film (represented as probe card 12) [see column 6 lines 27-28], the plurality of electrodes (16)being exposed through the resin film (12) [see fig. 1], inserting the wafer (10) into a burn-in apparatus (represented as burn-in cassette), testing the plurality of circuit elements [not shown] for electrical functions in the burn-in apparatus (burn-in cassette) through the plurality of electrodes (16) and dividing the wafer (10) [see fig. 3 with scribe lines dividing each semiconductor device] into the plurality of semiconductor device [not

number but shown in fig. 3]. However, he does not disclose the wafer expose to air as claimed. Budnaitis et al disclose [see Figs. 2-3] providing a semiconductor wafer (1) with a wafer surface having a plurality of circuit elements (chips 2) formed thereon, inserting the wafer (1) into a burn-in apparatus (6) wherein the wafer (1) is exposed to convective air in the burn-in apparatus (6) [see column 8 lines 41-54]. Further, Budnaitis et al teach that the addition of the wafer exposed to air is advantageous because it provides temperature control of the wafer during testing in the burn-in apparatus. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Nakata et al by adding means to blow air on the wafer as taught by Budnaitis in order to control the temperature of the wafer during testing in the burn-in apparatus.

Regarding claims 22, Nakata inherently discloses dividing the wafer after testing [see fig. 3].

Regarding claims 23 and 25, Nakata discloses mounting the wafer (10) on a circuit board (represented as wiring board 13) with an elastic sheet or film (represented as conductive rubber 21) interposed there between including electrically connecting wiring circuit [nit number but shown in fig. 1] on the circuit board (13) to the electrodes (16) on the wafer (10) through bump electrode (17) in the film (21).

Regarding claims 24 and 26, Nakata discloses disposing over the wafer (10) a holding plate (represented as first sealed member 15 and second sealed member 25) having a through hole (26) and pressing the wafer (10) on the circuit board (13) with the holding plate (15 and 25) [see column 6 line 56- column 7 line 54].

Regarding claim 27, Nakata discloses forming a plurality of solder balls as the electrodes (17) [see fig. 1].

Regarding claims 42-43, Budnaitis et al disclose [see Figs. 2-3] providing the convective air (hot or cold) over the wafer (1) through a through hole [see column 8 lines 41-52].

Regarding claim 44, Nakata et al discloses [see fig. 1] a method of manufacturing probe card of a wafer burn-in cassette comprising preparing a semiconductor wafer (10) with a first surface and a second surface, the second surface being opposite to the first surface, wherein the first surface has a plurality of circuit elements [not shown] formed thereon [see column 3 lines 27-30 and column 6 lines 25-26], forming a plurality of electrodes (16) on the first surface, the electrodes (16) being connected to the circuit elements [see column 6 lines 30-31], inserting the wafer (10) into a burn-in apparatus (represented as burn-in cassette), testing the plurality of circuit elements [not shown] for electrical functions in the burn-in apparatus (burn-in cassette) through the plurality of electrodes (16) and dividing the wafer (10) [see fig. 3 with scribe lines dividing each semiconductor device] into the plurality of semiconductor device [not number but shown in fig. 3]. However, he does not disclose the wafer expose to air as claimed. Budnaitis et al disclose [see Figs. 2-3] providing a semiconductor wafer (1) with a wafer surface having a plurality of circuit elements (chips 2) formed thereon, inserting the wafer (1) into a burn-in apparatus (6) wherein the wafer (1) is exposed to convective air in the burn-in apparatus (6) [see column 8 lines 41-52]. Further, Budnaitis et al teach that the addition of the wafer exposed to air is advantageous because it provides temperature control of the wafer during testing in the burn-in apparatus. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Nakata et al by adding means to blow air on the

wafer as taught by Budnaitis et al in order to control the temperature of the wafer during testing in the burn-in apparatus.

Regarding claims 45, Nakata inherently discloses dividing the wafer after testing [see fig. 3].

Regarding claims 46 and 48, Nakata discloses mounting the wafer (10) on a circuit board (represented as wiring board 13) with an elastic sheet or film (represented as conductive rubber 21) interposed there between including electrically connecting wiring circuit [nit number but shown in fig. 1] on the circuit board (13) to the electrodes (16) on the wafer (10) through bump electrode (17) in the film (21).

Regarding claims 47 and 49, Nakata discloses disposing over the wafer (10) a holding plate (represented as first sealed member 15 and second sealed member 25) having a through hole (26) and pressing the wafer (10) on the circuit board (13) with the holding plate (15 and 25) [see column 6 line 56- column 7 line 54].

Regarding claim 50, Nakata discloses forming a plurality of solder balls as the electrodes (17) [see fig. 1].

Regarding claims 51-52, Budnaitis et al disclose [see Figs. 2-3] providing the convective air over the wafer (1) through a through hole [see column 8, lines 41-52].

Conclusion

4. Applicant's arguments with respect to claims 21-27 and 42-52 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (703) 305-1653. The examiner can normally be reached on M-F (9:00-3:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Jermele M. Hollington
Examiner
Art Unit 2829

JMH
April 23, 2003

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